The background of the cover features a series of horizontal, rectangular cross-sections of a 3D integrated circuit stack, showing various layers and structures in shades of red and black. The top section shows a more complex, multi-layered structure, while the subsequent sections show simpler, more uniform layers.

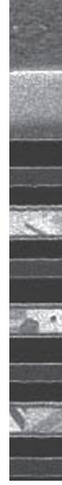
3D INTEGRATION for VLSI SYSTEMS

edited by
Chuan Seng Tan
Kuan-Neng Chen
Steven J. Koester





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Preface

Three-dimensional (3D) integration has emerged as a critical performance enabler for integrated circuits, at a time when the microelectronics industry is faced with unprecedented scaling barriers, which have arisen both due to fundamental physics and economic constraints. 3D integration provides a mechanism for space transformation of the traditional planar implementation of integrated circuits into three-dimensional space. It therefore provides a pathway to extend geometrical scaling for further performance enhancement (“More Moore”), as well as provide functional diversification (“More than Moore”) to improve higher-level system operation. At its core, 3D integration is simply the process of vertically stacking of circuits and forming electrical connections between them. Despite this seemingly simple concept, however, 3D integration involves significant development of many new technologies, from the basic processes and materials issues involved, to new approaches to system architectures, and it is the status and progress in these new areas that provide the focus of this book.

The advent of 3D integration is a direct result of relentless research in academia, research laboratories, and industry over the last 10 years. Today, 3D integration exists as a diverse set of stacking and vertical interconnection technologies that can take a multitude of forms, with the precise implementation depending on the applications. At the time of this writing, commercial 3D products already exist, including small form factor image sensors that include through silicon vias (TSV), and several announcements of future products, including 3D memory chips, have been made.

The concept of this book on 3D technology dates back to more than two years ago. At that time, an increasing number of publications and conferences had started to focus on 3D integration. At the end of an IEEE-sponsored International Workshop on Next Generation Electronics in Tainan, Taiwan, in November 2008, Pan Stanford Publishing (PSP) identified 3D integration as an important topic for book publication. While a few reference books on this emerging field already existed, there was an urgent need to highlight more recent developments in a new book and the idea of this book was formed. Given the many varieties of 3D integration technologies and its large span in the semiconductor supply chain, we decided to edit a book with contributions from experts in academia, research laboratories, and industry. After careful planning, we identified and invited chapter contribution from an impressive line-up of highly qualified researchers. It took more than one full year for planning, writing, and editing.

The objective of this book is to present novel ideas in pre-packaging wafer-level 3D integration technologies. The book covers process technologies such as wafer bonding, through silicon via (TSV), wafer thinning and handling, infrastructures, integration schemes, design as well as providing a succinct

outlook. All process technologies are carefully described and potential applications are listed. Technical challenges are also highlighted. This book is particularly beneficial to researchers or engineers who are already working or are beginning to work on 3D technology.

This book would not have been possible without a team of highly qualified and dedicated people. We are particularly grateful to Stanford Chong of PSP for initiating this undertaking and for providing his support. Rhamie Wahap and dedicated editorial staff at PSP worked alongside with us and provided us with the necessary editorial support. The three co-editors were funded for many years through the MARCO and DARPA funded Interconnect Focus Center (IFC) as well as the DARPA funded 3D IC Program; our 3D technology platform research, and this book, would not have been possible without this extended research support.

C.S. Tan is immensely grateful for the unfailing love and support from his wife, Lee Peng, without whom this book would not have been possible. He is currently supported by a Nanyang Assistant Professorship at the Nanyang Technological University. His research is generously supported by a grant from the Semiconductor Research Corporation (SRC), USA, through a subcontract from the Interconnect and Packaging Center at Georgia Institute of Technology, a seedling fund from Defence Advanced Research Program Agency (DARPA), USA, as well as the Defence Science and Technology Agency (DSTA) in Singapore. K.N. Chen would like to acknowledge funding supports from the National Science Council, Taiwan, as well as 3D IC research supports from the National Chiao Tung University, IBM T.J. Watson Research Center, and Massachusetts Institute of Technology. S. J. Koester is gratefully with support from the University of Minnesota.

Last but not least, we are extremely thankful to authors who accepted our invitation and contributed chapters to this book. We hope that the readers will find this book useful in their pursuit of 3D technology. Please do not hesitate to contact us if you have any comments or suggestions.

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